Amendments to the Claims:

1. (Currently Amended) A method for performing technology mapping, the method comprising:

a) receiving a design ~~that is not bounded to a particular technology~~;

b) repeatedly:

selecting from the design a candidate sub-network~~,~~ ;

identifying at least one replacement sub-network from a storage structure that stores replacement sub-networks; and

replacing the selected candidate sub-network in the design with the replacement sub-network~~.~~ ;

~~c)~~ wherein at least ~~each of a first set of replacement sub-networks have~~ a particular one of the replacement sub-networks has multiple circuit elements, wherein ~~each~~ at least one of the multiple circuit elements ~~of a first set replacement sub-network~~ of the particular replacement sub-network is independently selectable by the method in a later iteration of the method for inclusion in a candidate sub-network.

2. (Original) The method of claim 1, wherein identifying the replacement sub-network comprises:

generating a parameter based on a set of output functions performed by the selected candidate sub-network, wherein the parameter identifies the replacement sub-network.

3. (Original) The method of claim 2 further comprising: using the parameter to retrieve the replacement sub-network from the storage structure.

4. (Original) The method of claim 2, wherein the set of output functions includes only one output function.

5. (Original) The method of claim 2, wherein the set of output functions includes one or more output functions.

6. (Original) The method of claim 1 further comprising:

terminating the repetitions once a stopping criteria is reached.

7. (Currently Amended) The method of claim 6, wherein the received design is not bounded to a particular technology and includes a plurality of circuit elements, ~~and~~ the sub-networks are formed by circuit elements, and the storage structure stores replacement sub-networks that are bound to the technology, the method further comprising:

after terminating the repetitions, traversing the design to identify circuit elements that are not bound to the technology ~~library~~;

for each identified circuit element, attempting to identify a replacement sub-network that is stored in the storage structure; and

if at least one replacement sub-network for an identified circuit element is identified, replacing the circuit element in the design with the identified replacement sub-network.

8. (Original) The method of claim 7, wherein if more than one replacement sub-networks are identified for a circuit element, selecting one of the replacement sub-networks and replacing the circuit element with the selected replacement sub-network.

9. (Cancelled)

10. (Original) The method of claim 7, wherein each circuit element performs a function, wherein if no replacement sub-network is identified for an identified circuit element, decomposing the function of the circuit element into a set of functions, and then attempting to identify a set of replacement sub-networks in the storage structure that perform the set of functions.

11. (Cancelled)

12. (Cancelled)

13. (Original) The method of claim 1 further comprising:

before replacing the candidate sub-networks with the replacement sub-networks, evaluating whether to replace the selected candidate sub-network with the replacement sub-network,

wherein certain candidate sub-networks are replaced by replacement sub-networks based on the evaluation,

wherein certain candidate sub-networks are not replaced based on the evaluations.

14. (Original) The method of claim 13, wherein the evaluating comprises computing a cost function.

15. (New) A method for performing technology mapping on an initial design that is not bounded to a particular technology, the method comprising:

a) selecting from the design a first candidate sub-network;

b) replacing the first candidate sub-network in the design with a first replacement sub-network, the first replacement sub-network being stored in a storage structure that stores replacement sub-networks that are bound to the technology, wherein the first replacement sub-network is comprised of multiple circuit elements, at least one circuit element being independently selectable by the method in a later iteration of the method for inclusion in a candidate sub-network.

16. (New) The method of claim 15 further comprising:

c) selecting from the design a second candidate sub-network that includes at least one but not all circuit elements of the first replacement sub-network; and

d) replacing the second candidate sub-network in the design with a second replacement sub-network, the second replacement sub-network being stored in the storage structure.

17. (New) A method for performing technology mapping on an initial design that is not bounded to a particular technology, the method comprising:

a) selecting from the design a first candidate sub-network;

b) replacing the first candidate sub-network in the design with a first replacement sub-network, the first replacement sub-network being stored in a storage structure that stores replacement sub-networks that are bound to the technology, wherein the first replacement sub-network is comprised of multiple circuit elements;

c) selecting from the design a second candidate sub-network that includes at least one but not all circuit elements of the first replacement sub-network; and

d) replacing the second candidate sub-network in the design with a second replacement sub-network stored in the storage structure.

18. (New) The method of claim 17, further comprising:

before replacing the first candidate, identifying the first replacement sub-network from the storage structure; and

before replacing the second candidate, identifying the second replacement sub-network from the storage structure.

19. (New) The method of claim 17, further comprising :

repeatedly:

selecting from the design a particular candidate sub-network; and

replacing the particular candidate sub-network in the design with a particular replacement sub-network.

20. (New) The method of claim 19, wherein the received design includes a plurality of circuit elements, the method further comprising:

terminating the repetitions;

traversing the design to identify circuit elements that are not bound to the technology; and

replacing at least one identified circuit element with a replacement sub-network stored in the storage structure.

21. (New) A computer readable medium that stores a computer program for performing technology mapping on an initial design that is not bounded to a particular technology, the computer program comprising sets of instructions for:

a) selecting from the design a first candidate sub-network;

b) replacing the first candidate sub-network in the design with a first replacement sub-network, the first replacement sub-network being stored in a storage structure that stores replacement sub-networks that are bound to the technology, wherein the first replacement sub-network is comprised of multiple circuit elements;

c) selecting from the design a second candidate sub-network that includes at least one but not all circuit elements of the first replacement sub-network; and

d) replacing the second candidate sub-network in the design with a second replacement sub-network stored in the storage structure.

22. (New) The computer readable medium of claim 19, further comprising sets of instructions for:

before replacing the first candidate, identifying the first replacement sub-network from the storage structure; and

before replacing the second candidate, identifying the second replacement sub-network from the storage structure.

23. (New) The computer readable medium of claim 19, further comprising sets of instructions for:

repeatedly:

selecting from the design a particular candidate sub-network; and

replacing the particular candidate sub-network in the design with a particular replacement sub-network.

24. (New) The computer readable medium of claim 23, wherein the received design includes a plurality of circuit elements, further comprising sets of instructions for:

terminating the repetitions;

traversing the design to identify circuit elements that are not bound to the technology; and

replacing at least one identified circuit element with a replacement sub-network stored in the storage structure.

Amendments to the Drawings:

Attached are four sheets of drawings that include changes to Figures 6B, 14, 22B, and 22C. These sheets replace the original four sheets that included Figures 6B, 14, 22B, and 22C. The Examiner is respectfully requested to approve the amended drawings.